**Experiment 1: Data representation**

**Objective:**

1. To illustrate the concept of data representation

Theory:

**Data representation** refers to the way data is formatted, stored, processed, and transmitted in a computer system. Computers work with electrical signals that can be either "on" or "off," which is typically represented using binary numbers (0s and 1s). The different types of data representation are:

* Binary
* Hexadecimal
* Octal
* 1’s and 2’s complement

**Algorithm:**

i. Start

ii. Initialize a function to find binary 1’s and 2’s complement, hexadecimal, octal

equivalent of number

iii. Input a number to be converted

iv. Find the equivalent numbers

v. Print the binary 1’s and 2’s complement, hexadecimal and octal equivalent

numbers

vi. Stop

**Source code:**

#include<stdio.h>

int conversion(int num, int base)

{

int rem;

if (num == 0)

{

return 1;

}

else

{

rem = num % base;

conversion(num / base, base);

if (base == 16 && rem >= 10)

{

printf("%c", rem + 55);

}

else

{

printf("%d", rem);

}

}

}

int main()

{

int num;

printf("Enter the number: ");

scanf("%d", &num);

if(num!=0)

{

printf("The result Binary = ");

conversion(num, 2);

printf("\n");

printf("The result Hexadecimal = ");

conversion(num, 16);

printf("\n");

printf("The result Octal = ");

conversion(num, 8);

printf("\n");

}

else

{

printf("The binary number is=O\n");

printf("The hexadecimal number is=O\n");

printf("The octal number is=O\n");

}

}

Output:

**A screenshot of a computer

Description automatically generated**

**Source code:**

#include <stdio.h>

char onesComplement( char num)

{

return ~num;

}

char twosComplement( char num)

{

return onesComplement(num) + 1;

}

void printBinary( char num)

{

for (int i = 4; i >= 0; i--)

{

printf("%d", (num >> i) & 1);

}

}

int main()

{

char num;

printf("Enter an 4-bit number: ");

scanf("%d", &num);

unsigned char onesComp = onesComplement(num);

unsigned char twosComp = twosComplement(num);

printf("Original number: %d\n", num);

printf("Binary representation of original number: ");

printBinary(num);

printf("\n");

printf("Binary representation of 1's complement: ");

printBinary(onesComp);

printf("\n");

printf("Binary representation of 2's complement: ");

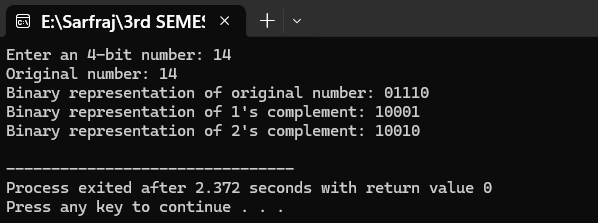
printBinary(twosComp);

printf("\n");

return 0;

}

Output:



**Experiment 2: Data overflow**

**Objective:**

1. To understand the concept of data overflow

**Theory:**

Overflow occurs when an arithmetic operation or a memory allocation exceeds the capacity of the data type or storage that is available. There are specific conditions under which overflow happens, depending on the type of operation and the data type being used.

**Condition for overflow:**

((AS==BS) &(AS==RS) || (AS! =BS))

{

NO overflow, display result;

}

**Algorithm:**

i. Start

ii. Observe carry into the sign bit position & carry out the sign bit position

iii. If the two carry aren’t equal, overflow should be detected

iv. If the two carry are applied to an X-OR gate overflow will be detected when

output of gate is 1.

v. Stop

**Source code:**

#include <stdio.h>

int main()

{

int num1,num2,r,as,bs,rs;

printf("Enter two numbers:");

scanf("%d%d", &num1,&num2);

r=num1+num2;

as=(num1>>4)&1;

bs=(num2>>4)&1;

rs=(r>>4)&1;

if(((as==bs)&&(as==rs))||(as!=bs))

{

printf("\No Overflow \n Result=%d",r);

}

else

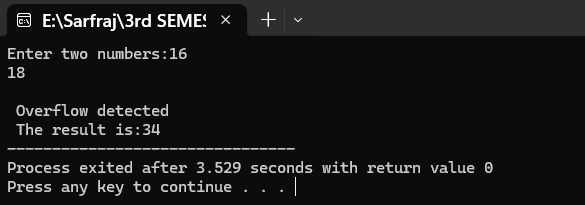
{

printf("\n Overflow detected\n The result is:%d",r);

}

}

**Output:**

****

**Experiment 3: Introduction to VHDL**

**Objective:**

1. To implement the Basic gates and universal gates using VHDL

**Theory:**

**VHDL** stands for (**VHSIC Hardware Description Language)**. It is a **hardware description language** used to model and simulate digital systems, such as circuits and systems designed using **VLSI (Very-Large-Scale Integration)** technology. VHDL is used primarily in **designing hardware** and describing its behavior, structure, and timing. In VHDL, entity is used to describe a hardware module. An entity can be described

using:

i. Entity declaration

ii. Architecture

iii. Configuration

iv. Package declaration

v. Package body

**Entity Declaration**:

It defines the name, input/output signals and modes of hardware module.

Syntax:

entity entity\_name is

port declaration;

end entity\_name;

Architecture:

Can be described using structural, data flow, behavior or mixed type.

Syntax:

architecture architecture\_name of entity\_name is

architecture architecture\_declarative part;

begin

statements;

end architecture\_name;

logic operation: N

**Experiment i: Introduction to VHDL**

**Objective:**

1. To implement the and gates using VHDL

**Theory:**

An AND gate is a basic digital logic gate that implements logical conjunction—meaning it outputs true (or 1) only if all its inputs are true (or 1). If at least one input is false (or 0), the output will be false (or 0). The AND gate is one of the fundamental building blocks in digital electronics.

**Truth Table for AND Gate:**

|  |  |  |
| --- | --- | --- |
| **Input A** | **Input B** | **Output (A AND B)** |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

**Source code:** For and gate

**Testbench:**

-- Testbench for AND gate

library IEEE;

use IEEE.std\_logic\_1164.all;

entity testbench is

-- empty

end testbench;

architecture tb of testbench is

-- DUT component

component and\_gate is

port(

a: in std\_logic;

b: in std\_logic;

q: out std\_logic);

end component;

signal a\_in, b\_in, q\_out: std\_logic;

begin

-- Connect DUT

DUT: and\_gate port map(a\_in, b\_in, q\_out);

process

begin

a\_in <= '0';

b\_in <= '0';

wait for 10 ns;

a\_in <= '0';

b\_in <= '1';

wait for 10 ns;

a\_in <= '1';

b\_in <= '0';

wait for 10 ns;

a\_in <= '1';

b\_in <= '1';

wait for 10 ns;

-- Clear inputs

a\_in <= '0';

b\_in <= '0';

wait for 20 ns;

end process;

end tb;

**Architecture:**

-- Simple AND gate design

library IEEE;

use IEEE.std\_logic\_1164.all;

entity and\_gate is

port(

a: in std\_logic;

b: in std\_logic;

q: out std\_logic);

end and\_gate;

architecture rtl of and\_gate is

begin

process(a, b) is

begin

q <= a and b;

end process;

end rtl;

**Output:**

**A screenshot of a video game

Description automatically generatedExperiment ii: Half adder**

**Objective:**

1. To implement the Half adder using VHDL

**Theory:**

A half adder is a basic digital circuit used to add two single-bit binary numbers. It has two inputs, typically labeled A and B, and two outputs: the sum (S) and the carry (C).

* **Sum (S)**: This is the result of the bitwise addition of A and B, without considering any carry from a previous operation. It can be found using the XOR (exclusive OR) operation.
* **Carry (C)**: This is the carry-out bit, which is generated when both A and B are 1, meaning there is an overflow into the next higher bit. It can be found using the AND operation.

**Truth table**:

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | Sum(S) | Carry(C) |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

**Source code:**

**Testbench:**

-- Testbench for halfadder gate

library IEEE;

use IEEE.std\_logic\_1164.all;

entity testbench is

-- empty

end testbench;

architecture tb of testbench is

-- DUT component

component halfadder\_gate is

port(

a: in std\_logic;

b: in std\_logic;

sum: out std\_logic;

carry:out std\_logic);

end component;

signal a\_in, b\_in, sum\_out, carry\_out: std\_logic;

begin

-- Connect DUT

DUT: halfadder\_gate port map(a\_in, b\_in, sum\_out, carry\_out);

process

begin

a\_in <= '0';

b\_in <= '0';

wait for 10 ns;

a\_in <= '0';

b\_in <= '1';

wait for 10 ns;

a\_in <= '1';

b\_in <= '0';

wait for 10 ns;

a\_in <= '1';

b\_in <= '1';

wait for 10 ns;

-- Clear inputs

a\_in <= '0';

b\_in <= '0';

wait for 20 ns;

end process;

end tb;

**Architecture:**

-- Simple halfadder gate design

library IEEE;

use IEEE.std\_logic\_1164.all;

entity halfadder\_gate is

port(

a: in std\_logic;

b: in std\_logic;

sum: out std\_logic;

carry:out std\_logic);

end halfadder\_gate;

architecture rtl of halfadder\_gate is

begin

process(a, b) is

begin

sum <= a xor b;

carry <= a and b;

end process;

end rtl;

**Output:**

**A screenshot of a game

Description automatically generated**

**Experiment iii: Full adder**

**Objective:**

1. To implement the Full adder using VHDL

**Theory:**

A **Full Adder** is a digital circuit that computes the sum of three binary inputs: two **operands** and a **carry-in** bit. It produces a **sum** and a **carry-out** bit.

The Full Adder is an extension of the **Half Adder**, which only adds two binary bits. In the Full Adder, we also consider a carry from the previous addition, making it more suitable for multi-bit binary addition, such as adding numbers in computer arithmetic. The output of full adder are:

1. **Sum (S)** (The result of adding A, B, and Carry-in)
2. **Carry-out (Cout)** (Carry to the next bit position)

Truth table:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **Cin** | **Sum(S)** | **Carry(Cout)** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

**Source code:**

-- Testbench for fulladder gate

library IEEE;

use IEEE.std\_logic\_1164.all;

entity testbench is

-- empty

end testbench;

architecture tb of testbench is

-- DUT component

component fulleladder\_gate is

port(

a: in std\_logic\_vector(3 downto 0);

b: in std\_logic\_vector(3 downto 0);

c:in std\_logic;

sum: out std\_logic\_vector(3 downto 0);

carry:out std\_logic);

end component;

signal a\_in,b\_in:std\_logic\_vector, c\_in:std\_logic;

signal sum\_out:std\_logic\_vector(3 downto 0),carry\_out:std\_logic;

begin

-- Connect DUT

DUT: fulladder\_gate port map(a\_in, b\_in, c\_in, sum\_out, carry\_out);

process

begin

a\_in <= '0';

b\_in <= '0';

c\_in <= '0';

wait for 10 ns;

a\_in <= '0';

b\_in <= '0';

c\_in <= '1';

wait for 10 ns;

a\_in <= '0';

b\_in <= '1';

c\_in <= '0';

wait for 10 ns;

a\_in <= '0';

b\_in <= '1';

c\_in <= '1';

wait for 10 ns;

a\_in <= '1';

b\_in <= '0';

c\_in <= '0';

wait for 10 ns;

a\_in <= '1';

b\_in <= '0';

c\_in <= '1';

wait for 10 ns;

a\_in <= '1';

b\_in <= '1';

c\_in <= '0';

wait for 10 ns;

a\_in <= '1';

b\_in <= '1';

c\_in <= '1';

wait for 10 ns;

-- Clear inputs

a\_in <= '0';

b\_in <= '0';

c\_in <= '0';

wait for 20 ns;

end process;

end tb;

**Architecture:**

-- Simple fulladder gate design

library IEEE;

use IEEE.std\_logic\_1164.all;

entity fulladder\_gate is

port(

a: in std\_logic;

b: in std\_logic;

c: in std\_logic;

sum: out std\_logic;

carry:out std\_logic);

end fulladder\_gate;

architecture rtl of fulladder\_gate is

begin

process(a, b, c) is

begin

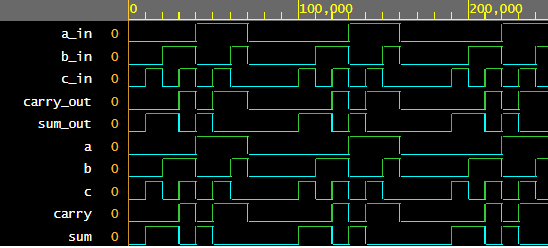
sum <= a xor b xor c;

carry <= (a and b) or (a and c) or (b and c);

end process;

end rtl;

**Output:**

****

**Experiment iv: 4-bit parallel adder**

**Objective:**

1. To implement the 4-bit parallel adder using VHDL

**Theory:**

A **4-bit parallel adder** is a digital circuit that adds two 4-bit binary numbers simultaneously, producing a 4-bit sum and a carry-out bit. It is made up of multiple **full adders** connected in parallel. Each full adder in the circuit adds corresponding bits of the two 4-bit inputs, along with any carry from the previous stage.

**Architecture:**

-- Simple paralleladder gate design

library IEEE;

use IEEE.std\_logic\_1164.all;

entity paralleladder\_gate is

port(

a: in std\_logic\_vector(3 downto 0);

b: in std\_logic\_vector(3 downto 0);

c: in std\_logic;

sum: out std\_logic\_vector(3 downto 0);

carry:out std\_logic);

end paralleladder\_gate;

architecture rtl of paralleladder\_gate is

begin

process(a, b, c) is

variable temp: std\_logic;

begin

temp:= c;

for i in 0 to 3 loop

sum(i) <= a(i) xor b(i) xor temp;

temp:=(a(i) and B(i)) or (temp and a(i)) or (temp and b(i));

end loop;

carry<=temp;

end process;

end rtl;

**Source code:**

-- Testbench for paralleladder gate

library IEEE;

use IEEE.std\_logic\_1164.all;

entity testbench is

-- empty

end testbench;

architecture tb of testbench is

-- DUT component

component paralleladder\_gate is

port(

a: in std\_logic\_vector(3 downto 0);

b: in std\_logic\_vector(3 downto 0);

c:in std\_logic;

sum: out std\_logic\_vector(3 downto 0);

carry:out std\_logic);

end component;

signal a\_in,b\_in:std\_logic\_vector(3 downto 0):=(others=>'0'); signal c\_in:std\_logic;

signal sum\_out:std\_logic\_vector(3 downto 0):= (others=>'0');

signal carry\_out:std\_logic;

begin

-- Connect DUT

DUT: paralleladder\_gate port map(a\_in, b\_in, c\_in, sum\_out, carry\_out);

process

begin

--test 1

a\_in <="0011";

b\_in <="1111";

c\_in <='0';

wait for 10 ns;

--test 2

a\_in <="0011";

b\_in <="1100";

c\_in <='1';

wait for 10 ns;

--test 3

a\_in<="0101";

b\_in <="1010";

c\_in <='1';

wait for 20 ns;

end process;

end tb;

**Output:**

**A computer screen shot of a black screen

Description automatically generated**

**Experiment v: Encoder**

**Objective:**

1. To implement encoder using VHDL

**Theory:**

An **encoder** is a digital circuit that converts data from one format or code to another, typically from a larger set of inputs to a smaller set of outputs. In the context of binary systems, an encoder is a device that converts an active input line into a binary code corresponding to that input.

For example, in a **binary encoder**, the number of output bits is fewer than the number of input lines. The encoder "encodes" the input into a binary number representing the position of the active input line.

**Architecture:**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity Encoder4\_2 is

Port ( a: in STD\_LOGIC\_VECTOR (3 downto 0);

b: out STD\_LOGIC\_VECTOR (1 downto 0));

end Encoder4\_2;

architecture rtl of Encoder4\_2 is

begin

process(a)

begin

if (a="0001") then

b <= "00";

elsif (a="0010") then

b <= "01";

elsif (a="0100") then

b <= "10";

elsif (a="1000") then

b <= "11";

else

b <= "ZZ";

end if;

end process;

end rtl;

**Source code:**

Encoder:

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

ENTITY Encoder\_test IS

END Encoder\_test;

ARCHITECTURE behavior OF Encoder\_test IS

COMPONENT Encoder4\_2

PORT (a: IN std\_logic\_vector(3 downto 0);

b: OUT std\_logic\_vector(1 downto 0)

);

END COMPONENT;

signal a: std\_logic\_vector(3 downto 0) := (others => '0');

signal b: std\_logic\_vector(1 downto 0);

BEGIN

uut: Encoder4\_2 PORT MAP (a => a,b => b);

process

begin

wait for 100 ns;

a <= "0000";

wait for 100 ns;

a <= "0001";

wait for 100 ns;

a <= "0010";

wait for 100 ns;

a <= "0100";

wait for 100 ns;

a <= "1000";

wait;

end process;

end;

**Output:**

A screenshot of a computer

Description automatically generated